

IN THE SPECIFICATION

*A1*  
Please Replace the Title with

MULTIPLE CHIP SEMICONDUCTOR ARRANGEMENT HAVING ELECTRICAL  
COMPONENTS IN SEPARATING REGIONS

In the Claims

Please amend Claims 1,3, 5, and 6. Please cancel Claims 2 and 4. Please add new

Claims 10-15.

A clean version of all the pending claims is submitted below:

*sub B1*  
*A2*  
1. (Amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated  
circuit chips thereon, such chips being separated by separating regions in the fractional portion of  
the wafer;

a plurality of voltage generators, each one being associated with, and adjacent to,  
a corresponding one of the chips.

*A3*  
3. (Amended) The semiconductor recited in claim 2 wherein each one of the voltage  
generators is disposed in the separating region.

*A4*  
5. (Amended) The semiconductor recited in claim 1 wherein each one of the voltage  
generators has an electrical contact and wherein the semiconductor further includes:

a dielectric member having an electrical conductor thereon, such electrical  
conductor being elevated above the regions in the fractional portion of the wafer and electrically  
connected to the plurality of electrical contacts of the plurality of chips to electrically

interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer.

sub  
B2  
A

6. (Amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

an electrical conductor electrically connecting the plurality of electrical selected one or ones of the electrical components to the chips with portions of the electrical conductor elevated above the regions in the fractional portion of the wafer and spanning the separating regions between the chips in the fractional portion of the wafer.

7. (Amended) The semiconductor recited in claim 6 wherein each set of electrical components includes a plurality of different electrical components.

sub  
B3  
A

10. (New) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of electrical components, each one being associated with, and adjacent to, a corresponding one of the chips; and

a fusible link electrically connecting a bus disposed in at least one of the plurality of integrated circuit chips and a corresponding one of the plurality of electrical components.

11. (New) The semiconductor recited in claim 10 wherein each one of the electrical components is disposed in the separating region.

12. (New) The semiconductor recited in claim 11 wherein the electrical components are voltage generators.

13. (New) The semiconductor recited in claim 12 wherein the voltage generators are interconnected by a conductor elevated above the regions in the fractional portion of the wafer.

*AS  
cont.* 14. (New) The semiconductor recited in claim 10 wherein the fusible link is disposed in disposed in at least one of the plurality of integrated circuit chips.

15. (New) The semiconductor recited in claim 12 wherein at least one of the voltage generators is coupled to more than one bus in corresponding ones of the plurality of integrated circuit chips.

---